MICROCRYSTALLINE SILICON GROWN ON LARGE-GRAINED POLYCRYSTALLINE SILICON FORMED BY ALUMINIUM-INDUCED CRYSTALLISATION

M. Birkholz, O. Nast, K. Kliefoth, E. Conrad, J. Rappich, P. Reinig, L. Elstner, W. Fuhs
Hahn-Meitner-Institut, Silizium-Photovoltaik, Kekuléstr. 5, D - 12489 Berlin
Phone +49-30-67053-309, Fax + 49-30-67053-333, E-mail: birkholz@hmi.de

ABSTRACT. We have deposited µc-Si films on aluminium-induced crystallised (AIC) silicon films and investigated their properties with respect to solar cell applications for the first time. According to Raman spectroscopy and X-ray diffraction, the initial amorphous growth phase, typically observed for µc-Si films, could be avoided on AIC substrates. However, the large-grained growth could not be induced from the AIC phase into the µc-Si film. Photovoltages of p^+/n contacts were measured by surface photovoltage measurements (SPV) to amount to 260 mV. The microcrystalline growth on large-grained poly-Si AIC material is discussed in the framework of a low surface mobility of silicon species due to the surface roughness of etched substrates and the low deposition temperature of 325°C.
Keywords: Microcrystalline Silicon –1 : Aluminium-Induced Crystallisation – 2

1. INTRODUCTION

The intended preparation of future thin-film silicon solar cells on large-area substrates like glass or stainless steel puts some restriction on the temperature of the preparation process. In order to avoid the substrate's mechanical deformation or interdiffusion between the substrate and the semiconducting layers, the process temperature must not exceed some hundred °C, which is less or equal than half the melting temperature of silicon, $T_M = 1683$ K. Growth of thin films in such a low temperature regime in general would only yield material of inferior crystallinity [1] and electronic quality. Therefore, CVD techniques are required for the low-temperature path, in which part of the thin-film-formation energy is transferred to the silicon species in the gas phase, and not solely via heating of the substrate. Such techniques are plasma-enhanced PECVD [2] and hot-wire CVD [3]. The growth of thin microcrystalline silicon µc-Si films on foreign substrates by these techniques proceeds through a set of different stages of crystalline ordering that are associated with an initial amorphous layer and the evolution of a preferred orientation [4]. The concept of the deposition on a highly crystalline Si seeding layer offers an alternative approach. One may hope to circumvent the initial and intermediate growth stages as observed on foreign substrates by directly depositing on silicon. Seeding layers have so far been prepared by laser crystallisation LC [5], solid phase crystallisation SPC [6] and just recently by aluminium-induced crystallisation AIC [7] of amorphous silicon films. In spite of the large body of literature on the preparation of seeding layers by these methods, only few reports have been given on the deposition of thin films upon such substrates.

This study deals with the deposition of undoped µc-Si films grown on p^+-Si seeding layers prepared by aluminium-induced crystallisation (AIC). The latter technique is based on an aluminium-induced layer exchange process of Al/*a*-Si layered structures. This process is conducted between 400 and 550 °C and leads to the formation a large-grained polycrystalline silicon film [8]. The method appears to be well suited for the low-temperature approach, since it avoids the strong heating of the substrate as it occurs in LC or SPC processes. The question arises, in how far the large-grained structure can be conserved during following µc-Si growth and what electronic properties the obtained interface will have. In order to elucidate these questions we have deposited µc-Si by electron-cyclotron resonance (ECR) CVD films on AIC layers. Structural properties were investigated by Raman spectroscopy and X-ray diffraction (XRD). The electronic properties of the junction were investigated by surface photovoltage measurement (SPV) in the range from 170 to 300 K. This is the first study on µc-Si films grown on AIC material and, therefore, aims at elucidating the potentials and the obstacles that are related to the growth mode of the µc-Si layer and the interface formation between both silicon films.

Regarding the possible use of AIC layers in thin-film silicon solar cells the most important restriction stems from its conduction type. Due to the intermixing of Al- and Si-phases during the process, the obtained silicon layer is always p^+-type exhibiting an Al concentration of about 10^{19} cm^{-3} at 400 - 500°C [9]. AIC films may, therefore, only be used as *p*-type layer in devices such as *p-i-n* (substrate) or *n-i-p* (superstrate). The more simple device is the *pin* configuration. In this case, the AIC process may be employed such that the following deposition of the *i*-layer is performed on a substrate/Al/Si system and, advantageously, the Al back contact is automatically formed by the AIC process. In the case of the *nip* configuration, the process yields the polycrystalline silicon layer directly on the holding structure which may either be glass or a TCO layer. The aluminium remains on top of the structure and has to be etched-off to proceed with the *i*- and *n*-type layer depositions. For this configuration the solar cell device may be illuminated through the glass to which the AIC *p*-layer is attached, while in the other case a reflecting Al prohibits this geometry. Therefore, the two configurations may be called substrate and superstrate configurations, respectively, Fig. 1. In the following we will only be concerned with the growth of µc-Si on AIC-Si intended for use as absorber layer in the substrate configuration.

2. PREPARATION

Aluminium-induced crystallisation was performed with a substrate/Al(300 nm)/*a*-Si (300 nm)/Al (150 nm) layer system. The Al and Si films were deposited using electron beam evaporation and dc magnetron sputtering, respectively. No additional substrate heating was applied in either deposition. Most of the layer systems were deposited on Corning 1737 F glass, some others on CZ-Si (100) 12-20 •cm. Prior to Al evaporation, the chamber was pumped down to typically 3×10^{-7} mbar. The deposition rate was set to 1.5 nm/s. For the deposition of the amorphous Si films an intrinsic Si target was sputtered

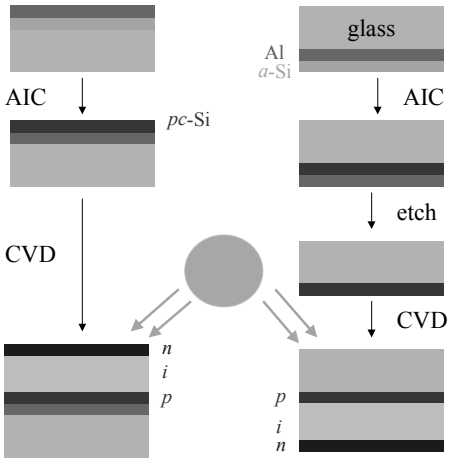

Figure 1: *Schemes of p-i-n (substrate) and n-i-p (superstrate) solar cells using AIC p^+-Si layers.*

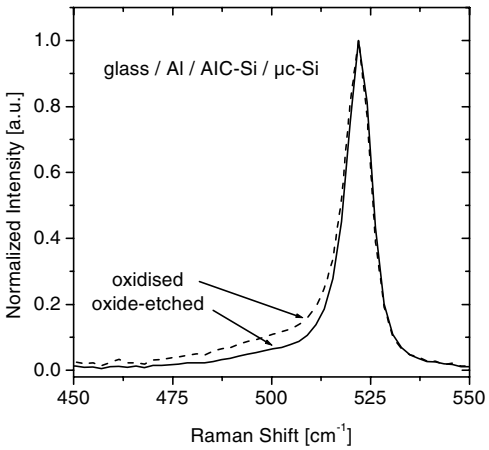

Figure 2: *Raman spectra of µc-Si films deposited on AIC. Dashed-line spectrum indicates deposition on electrochemically oxidised AIC films, while the solid line accounts for a sample for which the surface oxide was removed prior to CVD process*

with a power density of 1.9 W/cm² and a target-substrate distance of 50 mm in a pure 6×10^{-3} mbar Ar atmosphere. The base pressure of the vacuum system was typically 2×10^{-7} mbar. The samples were exposed to ambient air after the deposition of each layer. The Al/*a*-Si/Al trilayer system was isothermally annealed at 475°C for 120 min, leading to the exchange of the top Al film with the Si layer. During the Al-induced layer exchange process a poly-Si layer was formed replacing the former Al film. The newly formed layer system had a glass/Al/Al+(Si)/poly-Si sequence. The Al+(Si) layer resembles an Al matrix with residual Si imbedded in the form of Si crystallites. The overall layer exchange phenomenon is discussed in more details in these proceedings [9]. The particular layer structure used in this paper has recently been investigated by Nast and Hartmann [10]. The poly-Si film formed was of equal thickness as the original top Al layer. To avoid a possible Si-Al-O phase on the poly-Si surface that would have hampered the following µc-Si growth directly on AIC-Si, the poly-Si layer was electrochemically oxidised in ethylene-glycol containing H_2O according to Ref. [11]. The oxide layer formed was about 15 nm thick. The remaining organic solvent on the poly-Si surface was eliminated in a H_2SO_4 cleaning step for 5 s. The Si oxide film with all possible contamination on the top was selectively etched off in a 2% HF solution for 30 sec. Immediately before loading the poly-Si seeding layer into the CVD chamber the samples were finally HF dipped (2 %) for 5 s.

The deposition of µc-Si was performed with a plasma-enhanced electron-cyclotron resonance (ECR) CVD system that has been described previously [12]. The plasma was ignited from silane-hydrogen mixtures by coupling a 2.45 GHz microwave into the active ECR region of 875 G within two magnetic coils. The substrate temperature was set to 325 °C for all depositions reported in this work. The high-vacuum recipient exhibited base pressures in the range from $5\text{-}50 \times 10^{-8}$ Torr. Intentionally undoped µc-Si films as prepared in this system are found *n*-type. The same has been reported by other groups that also prepare in low-temperature CVD regimes. The *n*-type doping is generally attributed to the incorporation of oxygen from the residual gas phase. Recently, deposition conditions of the ECR CVD could be identified under which µc-Si films with a high degree of crystallinity and appropriate electronic properties could be prepared [13]. Dark conductivities σ_d in the 10^{-7} S/cm range and more than 10^2 larger photoconductivities σ_{ph} were obtained. In this work, the total pressure was 2.4 mTorr, a microwave of 800 W was applied and the flow rate of working gas H_2 and process gas SiH_4 were 30 sccm and 10 sccm, respectively. The deposition rate was 10 nm/min. It was tried to avoid the initial amorphous growth by employing high hydrogen dilution at the beginning of the deposition. We, therefore, step-wise increased the silane flow while leaving the H_2 flow constant. Some of the µc-Si films deposited by ECR onto AIC layers were moreover covered by n^+ layer prepared by conventional parallel-plate PECVD. This system was part of the same cluster tool as the ECR, with both chambers being connected to a central wafer handler. The sample transfer therefore could be performed without breaking the vacuum.

3. RAMAN SPECTROSCOPY; X-RAY DIFFRACTION AND PHOTOVOLTAGE MEASUREMENTS

Comparative Raman spectroscopy measurements were conducted to elucidate the initial growth behaviour of µc-Si. Raman spectra were recorded with a Dilor/ISA LabRAM 010 by using an Ar-ion laser excitation with $\lambda_0 = 457.9$ nm. For this wavelength the absorption length of µc-Si is about 50 nm [14]. µc-Si films of only 40 nm thickness were prepared in the same deposition run (i) onto the bare AIC Si film after HF etching and (ii) on the still electrochemically oxidised poly-Si surface. Figure 2 displays the two types of obtained Raman spectra that were baseline-corrected and normalised with respect to the maximum intensity of the LO/TO line of crystalline silicon at 521 cm^{-1}. Both spectra are composed of responses from the µc-Si film and underlying poly-Si material. The solid-line spectra were measured with samples subjected to a 30 s HF-etch in order to remove the oxide layer. In case of the dashed curve, the µc-Si deposition was performed on AIC-Si surfaces that were not HF-etched after the electrochemical oxidation. The analysis of the Raman spectra focuses on the amplitude at 480 cm^{-1} that indicates remaining amorphous or disordered Si phases in the sample. It is evident from the comparison that the solid-line spectra exhibit a reduced intensity at 480 cm^{-1} compared to the dashed-line spectra. It can be concluded that the growth of µc-Si of improved

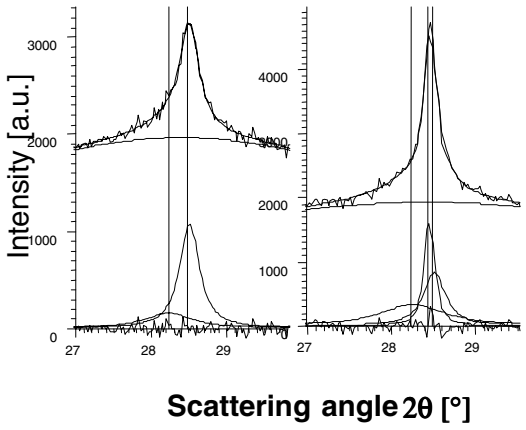

Figure 3*: (111) Bragg reflections from x-ray diffractograms of µc-Si on glass (left) and on glass/Al/AIC-Si (right). Bottom: single line shapes of fitted reflections.*

crystallinity does occur on AIC-Si when compared with the growth on a foreign oxide phase. It remains unanswered by Raman spectroscopy whether the effect is due to increased grain size or due to avoiding the initial amorphous phase.

X-ray diffractograms of µc-Si films on AIC and glass substrates were investigated, in order to examine whether the large-grain structure of the AIC film may be continued to govern the µc-Si growth, too. Measurements were performed with a Bruker D8 Advance diffractometer in symmetric •••• geometry and asymmetric grazing incidence diffraction. CuK• radiation (•.. = 1.5406 Å) was employed. Bragg reflections of µc-Si could well be fitted by Lorentzian line shape functions, while splitted Lorentzians have to be applied for reflections from the AIC phase. Figure 3 displays the (111) Si reflections of ECR-deposited µc-Si films on glass (left) and on AIC-Si on glass/Al (right). A lower-•• satellite reflex is typically observed for µc-Si films grown at low temperatures, indicating a stacking fault sequence in the [111] direction [15]. Therefore, the reflection of the µc-Si sample on glass had to be fitted with two lines of distinct peak centroids ••. (vertical lines) and FWHMs. The fit can be seen to account very well for the measured line profile. The same reflection is shown on the right-hand side of the figure for deposition on a AIC-Si substrate. In this case the regression had to be performed by three peaks, since the (111) lattice planes of the Si substrate adds up to the diffraction pattern. The total Bragg reflex could be fitted by a simple superposition of two peaks with the same line shape parameters as given above and a third line exhibiting FWHM values that are typically found for AIC material. Comparable results were obtained for higher Bragg reflections (*hkl*) and also in grazing incidence geometry (not shown here). It is therefore concluded that the grain structure of the µc-Si film is not influenced by the underlying AIC-Si film. The large-grain structure of AIC does not continue into the µc-Si film.

The electronic structure of the p^+/n interface as prepared by the combination of AIC and ECR CVD was investigated by surface photovoltage (SPV) measurements. It has been shown that the photovoltage U_{ph} as obtained in the SPV measurement compares directly with the build-in voltage or open-circuit voltage V_{oc} of a solar cell [16]. Therefore, this quantity appeared to be a reliable optimisation parameter for the p^+/n interface at this early stage of investigation. In the SPV measurement the change of band bending at the interface

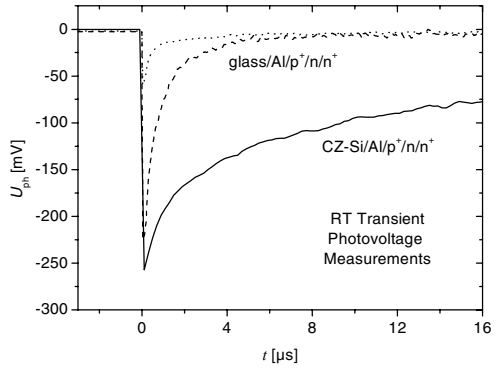

Figure 4: *Room-temperature SPV transients of two samples deposited on glass (top) and one sample deposited on CZ-Si.*

is studied by illuminating the sample with a short laser pulse and capacitively measuring the photovoltage transient. The sample is part of an artificial MIS structure, in which optically clear mica with a thickness of about 5 µm serves as the insulator, while the gate is formed by a TCO electrode. The optical stimulation proceeds by a 150 ns laser pulse at 900 nm causing a change of the charge distribution inside the space charge region during the dielectric relaxation time. For sufficiently high light intensities the bands are flattened and the maximum amplitude of the photovoltage transient reflects the build-in voltage, see Ref. [16] for a review of the method.

Figure 4 shows two SPV transients that were measured on Al/$p^+/n/n^+$ layer systems on Corning glass and on CZ-Si. The Al/p^+ system stands for the Al/Al+(Si)/poly-Si layer structure as described in the preparation section. The thickness of the ECR-grown n layer was 1150 nm. In this case the p^+/n contact was covered by a 100 nm thick n^+-Si layer deposited by PECVD. Since the critical interface is between the p^+ and the n layer, we expect the measured U_{ph} values from the SPV method to be yield information mainly from the p^+/n interface. The sample deposited on glass gives a maximum SPV amplitude of 220 mV. In addition, the figure displays an SPV transient measured for a layer system as deposited on a CZ-Si wafer. It should be noted again that a reflecting Al layer was situated between the p^+-AIC film and the CZ-Si substrate, such that the SPV signal could not be due to the Si wafer. The sample yielded an U_{ph} value of 260 mV. We interpret the substrate-dependence of the SPV transients by a reduced incorporation of contaminants from the substrate during wet-chemical processing. However, both measured U_{ph} values are small when compared with an expected build-in voltage of about 500 mV.

Temperature-dependent SPV measurements were also employed, from which one example is given in figure 5. The figure shows the SPV transients for a set of temperatures $T \leq 300$ K for a sample of structure glass/Al/AIC/µc-Si. It is realised from the plot that the maximum SPV amplitude does not change with decreasing temperature down to 175 K. The photovoltage U_{ph} is concluded to be independent of temperature in the investigated temperature interval. This has been typically observed for our samples. It may be assumed as an explanation for this effect that a fast recombination within the space charge region occurs on a much smaller time scale than the time resolution of the SPV transient. Also Fermi-level pinning due to a possible large interface defect density may account for a SPV signal independent from temperature. It would appear highly speculative trying to give an explanation of measured SPV data at this

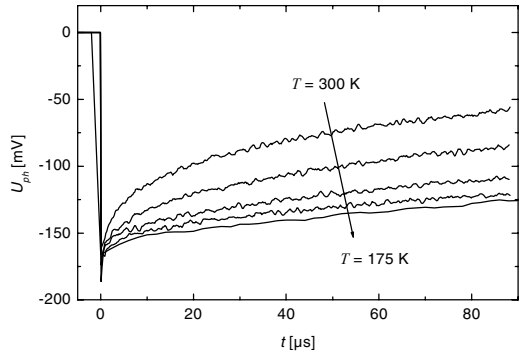

Figure 5: *SPV transients of a µc-Si/AIC sample deposited on glass for different temperatures*

early stage of investigations. More investigations are clearly necessary to improve our understanding from this particular Si-Si interface.

4. DISCUSSION AND CONCLUSION

The results of structural characterisation can be interpreted as follows. It has been shown by Raman spectroscopy that a profiled deposition process working with a high H_2 dilution in the beginning and successive increase of the silane flow leads to a film growth with improved crystallinity, if deposited on AIC-Si. On the other hand, XRD gave no indication for an increase of the average grain size for depositions on AIC material. It may be concluded from the combination of the results of both methods that the growth of µc-Si on AIC poly-Si can be performed without an initial amorphous layer. In this sense, an AIC substrate would in fact work as a seeding layer for polycrystalline silicon growth. On the other hand, a continued growth of the large-grained poly-Si forming the AIC material into the CVD-deposited film has not been observed yet. It appears not surprising under these circumstances that photovoltages of only 260 mV were obtained.

The use of AIC material appears promising for seeding layer applications because homo-epitaxial growth of silicon at low temperatures could only be demonstrated to occur on (100)-oriented wafers [17]. Since the AIC process gives a (100)-preferred oriented thin film [9] one may hope the growth on (100)-grains of the seeding layer to occur epitaxially and to dominate the crystallographic orientation of the total film. For a discussion of this approach, a model of both an H-terminated (100) CZ-Si wafer and an oxide-free AIC layer is displayed in Fig. 6. It is indicated in the figure that the surface conditioning is different for both substrates. Firstly, the electrochemically oxidised and HF-etched AIC surface will exhibit a significantly rougher surface than the CZ-Si wafer. Secondly, an H-terminated silicon surface may be conserved on a CZ-Si wafer for minutes, while this time will shrink significantly for rough silicon surfaces of varying orientation. Both phenomena will moreover cause a different surface mobility of silicon species on both substrates, which is one of the most important factors influencing the degree of crystallinity of the growing thin film. It should be pointed to the fact, moreover, that there exists only few studies were successful epitaxial growth on Si seeding layers has been claimed [6, 18]. In these studies, preparations were performed at temperatures of about 550°C and 600°C, which is significantly higher than the deposition temperature of 325°C used in this work. From these arguments we conclude that there still

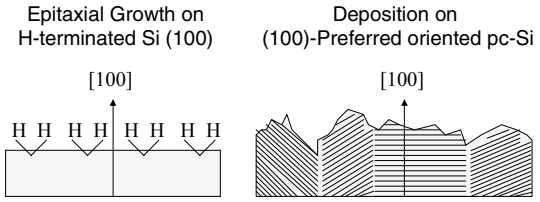

Figure 6: *Model of both an H-terminated (100)-oriented CZ-Si wafer and a AIC film having a (100)-preferred orientation.*

exists space for improvement for a continued large-grained growth from an AIC seeding layer. Especially methods for a low-roughness surface and a higher temperature regime should be considered in future work.

We thank G. Keiler, J. Krause, R. Linke, D. Patzek, B. Rabe, M. Schmidt and B. Steudel for technical assistance. This work was partially supported by the Bundesministerium für Wirtschaft.

REFERENCES

1. M. Ohring, *Materials Science of Thin Films* (Academic Press, San Diego, 1992), pp. 223.
2. R. Reif, W. Kern, in *Thin Film Processes*, edited by J. L. Vossen and W. Kern (Academic Press, Boston, 1991), **II**, p. 525.
3. R.E.I. Schropp, K.F. Feenstra, E.C. Molenbroek, H. Meiling, J.K. Rath, Phil. Mag. B **76**, 309 (1997).
4. M. Birkholz, B. Selle, E. Conrad, K. Lips, W. Fuhs, submitted to J. Appl. Phys. (2000).
5. R.B. Bergmann, G. Oswald, M. Albrecht, V. Gross, Solar Energy Materials and Solar Cells **46**, 147 (1997).
6. K. Yamamoto, A. Nakashima, T. Suzuki, M. Yoshimi, Jap. J. Appl. Phys. **33**, L1751 (1994).
7. O. Nast, T. Puzzer, L.M. Koschier, A.B. Sproul, S.R. Wenham, Appl. Phys. Lett. **73**, 3214 (1998).
8. O. Nast, S.R. Wenham, J. Appl. Phys., in print (2000).
9. O. Nast, T. Puzzer, C.T. Chou, M. Birkholz, this proceedings (PA2.4).
10. O. Nast, A.J. Hartmann, J. Appl. Phys., in print (2000).
11. S. Lust, J. Rappich, I. Sieber, W. Henrion, W. Fuhs, this proceedings (VA1.24).
12. P. Müller, E. Conrad, T.R. Omstead, P. Kember, in 13th EC Photovoltaic Solar Energy Conference, Nice, (Stephens & Associates, 1995), Vol. II, p. 1742.
13. M. Birkholz, E. Conrad, K. Lips, B. Selle, I. Sieber, S. Christiansen, W. Fuhs, in Mat. Res. Soc. Symp. Proc., R. W. Collins et al. (Eds.), in press (2000).
14. M. Schmidt, R. Krankenhagen, M. Poschenrieder, W. Henrion, I. Sieber, S. Grebner, S. Koynov, R. Schwarz, J. Non-Cryst. Sol. **198-200**, 923 (1996).
15. M. Hendriks, S. Radelaar, A.M. Beers, J. Bloem, Thin Sol. Films **113**, 59 (1984).
16. O.B. Aphek, L. Kronik, M. Leibovitch, Y. Sapira, Surf. Sc. **409**, 485 (1998).
17. J. Platen, B. Selle, I. Sieber, U. Zeimer, and W. Fuhs, in Mat. Res. Soc. Symp. Proc. **570**, 91 (1999).
18. R.B. Bergmann, *Siliziumsolarzellen auf Glassubstrat* (Max-Planck-Institut für Festkörperforschung, Stuttgart, 1997).